REMARKS

Claims 1-18 are all the claims pending in the application. By this Amendment, Applicant editorially amends claims 1, 2 and 18. The amendments to claims 1, 2 and 18 were made for reasons of precision of language and consistency, and do not narrow the literal scope of the claims and thus do not implicate an estoppel in the application of the doctrine of equivalents. The amendments to claims 1, 2 and 18 were not made for reasons of patentability.

I.   Preliminary Matters

As a preliminary matter, the Examiner is respectfully requested to acknowledge a claim for domestic priority by checking box 14 on the PTO form PTOL-326.

The Examiner requested that Applicant file an Information Disclosure Statement, enclosing references cited in the body of the Specification. Along with this response, Applicant files an Information Disclosure Statement with a list of cited references. Applicant thanks the Examiner for obtaining copies of the books: K.L. Mc Millan, Symbolic Model Checking, Kluwer Academic Publishers, 1993 and R.P. Kurshan, Computer Aided Verification of Coordinating Processes: The Automata-Theoretic Approach, Princeton Univ. Press 1995. Therefore, among the list of references cited, Applicant respectfully lists these two books but does not submit a copy of these two books.

II.   Summary of the Office Action

The Examiner objected to the Specification, Drawings and claims 2 and 4. Claims 1-13 stand rejected under 35 U.S.C. § 112, first paragraph and claims 1-15 and 18 under 35 U.S.C. § 112, second paragraph. In addition, the Examiner rejected claims 1, 15 and 16 under 35 U.S.C. §

102(b) and claims 1-4 under 35 U.S.C. § 103. Finally, the Examiner indicated that claim 17

contains allowable subject matter.

III.   Objection to the Specification

The Examiner objected to the title of the invention alleging that it is not descriptive (see

page 2 of the Office Action). Applicant amends the title to "Property-specific testbench

generation framework for circuit design validation by guided simulation." Therefore, Applicant

respectfully requests the Examiner to withdraw this objection.

IV.   Objection to the Drawings

The Examiner objected to the Drawings for failure to label Figures 1 and 17 as "prior art"

(see page 2 of the Office Action). The drawings have been amended to remedy this situation.

Replacement Drawings labeling Figure 1 with a legend -- prior art-- are accompanying this

response. As a result, the Examiner is respectfully requested to acknowledge receipt and indicate

approval of the drawing corrections in the next Patent office paper.

With respect to Figure 17, however, Applicant respectfully points out that it is not prior

art, as explained on page 29 of the Specification. Figure 17 includes a database with the state

transition priorities, which is one of many novel features of the present invention. Therefore, the

Examiner is respectfully requested to withdraw this objection to Figure 17.

V.   Objection to the Claims

The Examiner objected to claims 2 and 4 because of minor informalities (see page 3 of

the Office Action). The Examiner's pointing out with particularity, the aspects of the claims

thought to be indefinite is gratefully noted.

With respect to claim 2, a semi-colon was replaced with a colon, as shown in the attached Appendix. However, the Examiner has also objected to the claim because it recites "said generation", whereas it allegedly should recite "said generating" (see page 3 of the Office Action). It is respectfully submitted that the terms are not inconsistent within the meaning of MPEP § 608.01(m) nor does this terminology fails to inform one of ordinary skill in the art of the scope of the claim within the meaning of MPEP § 2173.05(e). It is, therefore, appropriate for the Examiner to withdraw this objection to claim 2. Otherwise, it is respectfully requested that the Examiner point out where in the MPEP such terminology is deemed to be inconsistent.

With respect to claim 4, the Examiner alleges that it should recite an "or" instead of an "and". However, it is respectfully pointed out that claim 4 recites "one *or more of*". In other words, one or more elements out of a group of elements can be chosen; the elements of the group are listed with an "and". That is, if for example, a claim is directed to choosing fruit, it may recite choosing one or more of bananas, oranges *and* apples. A banana and an apple may be chosen. Therefore, an "or" would impermissibly limit the scope of the claim. As such, it is appropriate and necessary for the Examiner to withdraw this objection to claim 4.

VI.   Claim Rejections under 35 U.S.C. § 112, first paragraph

Next, the Examiner rejected claims 1-13 under 35 U.S.C. § 112, first paragraph, alleging that the specification does not reasonably enable one of ordinary skill in the art with respect to "empty" v. "not-empty" witness graphs, as set forth in claim 1 (see page 3 of the Office Action). In support, the Examiner notes that page 28 of the Specification teaches pruning the witness graph until a final witness graph is achieved but that no empty witness graph is discussed (see page 3 of the Office Action).

For a discussion of an exemplary, non-limiting embodiment of an empty witness graph tree, see pages 17-18 of the Specification. In particular, the discussion of an illustrative, non-limiting witness graph generation begins on page 10 of the Specification. That is, an iterative refinement approach is followed for generation of a Witness Graph, where the start is from a very abstract model of the design, followed with performing deterministic analysis for pruning it, and then refining it to perform analysis again. The iterative process is repeated until a conclusive result or resource limitations are reached. This flow is shown within the dashed box in Fig. 4 – each of its components is described in detail (see last paragraph on page 10 of the Specification).

As shown in Fig. 4, one of the steps in generating a witness graph is determining whether a conclusive result may be achieved. An exemplary, non-limiting embodiment of this step is discussed on pages 17-18 of the Specification. As explained on these pages, if the property is determined as true or false, the witness graph is empty, e.g. if the initial state does not belong to the set *upper*, the property is false. If the property is false or true, then no existing paths are present. If it is determined that *no existing paths are present* or that *initial state does not belong to the set*, then clearly no paths for the witness graph can be generated, and as a result, the witness graph will be empty (e.g. Specification, page 27, second full paragraph). This discussion is presented by way of an example only and is not intended to limit the scope of the claims in any way.

Therefore, it is respectfully submitted that one of ordinary skill in the art is enabled as to when a witness graph is empty, as set forth in claim 1. It is appropriate and necessary for the Examiner to withdraw this rejection of the claims 1-13.

VII.   Claim Rejections under 35 U.S.C. § 112, second paragraph

Next, the Examiner rejected claims 1-13, 14, 15 and 18 under 35 U.S.C. § 112, second

paragraph for failing to particularly point out and distinctly claim the subject matter which

Applicant regards as the invention. The Examiner has issued a number of rejections under § 112,

second paragraph. In particular, the Examiner alleges that claim 1 is indefinite for reciting

"empty witness graph", "one or more properties" and for not reciting "pruning", claims 2 and 15

are indefinite for reciting "generating modules", claim 14 for reciting "completely simulated"

and claim 18 for insufficient antecedent basis.

In making the rejections, the Examiner provides various interpretations of the claims. It

is respectfully noted that there is no acquiescence to the inferences or presumptions drawn from

the Examiner's interpretations of the claims. Each of these rejections is addressed below.

A. Empty Witness Graph is Definite

In particular, the Examiner alleges that because the specification does not disclose an

empty witness graph, as set forth in claim 1, it is unclear how to interpret the claims (see page 4

of the Office Action). The Examiner's pointing out with particularity the aspect of the claim

thought to be indefinite is gratefully noted. Applicant traverses this rejection by respectfully

submitting that the Specification clearly teaches an illustrative, non-limiting embodiment of

having an empty witness graph as explained in § VI of this Amendment. Therefore, the

arguments presented in § VI apply with equal force herein. For at least these reasons, it is

appropriate and necessary for the Examiner to withdraw this rejection of claims 1-13.

B. Testing Properties Using Witness Graphs

Next, the Examiner rejects claim 1 for being indefinite as to how the witness graph can

include paths only demonstrating the property violation or property satisfaction (see page 4 of

the office action). In particular, the Examiner notes "that the witness graph would inherently

contain other paths demonstrating other properties." In this case, the Examiner alleges that

Applicant appears to be claiming multiple witness graphs or merely a portion of the witness

graph. Applicant does not acquiesce to any inferences or presumptions drawn from this

statement by the Examiner. However, Applicant amends claim 1 to further clarify the invention.

In particular, claim 1, as now amended, recites that a witness graph is generated for one of the

correctness properties. In view of this clarification, Applicant respectfully requests the Examiner

to withdraw this rejection of claims 1-13.

C. Lack of Pruning Does Not Render Claim 1 Indefinite

Moreover, the Examiner alleges that because pruning is not defined, that any prior art

generating testbench until a conclusive result of property meets the limitations of claim 1 (see

pages 4-5 of the Office Action). Applicant does not acquiesce to any inferences or presumptions

drawn from this statement by the Examiner. The Examiner is attempting to impermissibly limit

the scope of the claim.

For example, an illustrative, non-limiting embodiment of the present invention teaches

that in general, for a property concerning a single path (with the existential path quantifier), the

generated vectors must be directed toward finding a witness. For a property concerning all paths

(with the universal path quantifier), the generated vectors must be directed toward finding a

counter-example. The exemplary witness graph is used to denote the collection of states and

transitions in the design which are useful for enumerating witnesses or counter-examples for the

required property (page 9 of the Specification). The exemplary final witness graph will be empty

if a conclusive result is reached (property proven true or false). Alternatively, the exemplary

final witness graph will contain a number of paths with witnesses or counter examples, and this

illustrative final witness graph will be generated once the resource limitations are reached (page

10-11 of the Specification).

In short, an exemplary, non-limiting embodiment teaches generating a witness graph,

which may be empty if during generation a conclusive result of the property is established. In

particular, if the property refers to a universal path qualification, the conclusive result is property

satisfaction but if the property refers to an existential path qualification then conclusive result is

property violation. On the other hand, a witness graph may comprise a number of paths if the

result is inconclusive. If property refers to universal path, then the witness graph will include

paths demonstrating only property violation. In contrast, if the property refers to an existential

path, the witness graph will comprise witnesses (paths demonstrating property satisfaction). The

testbench is automatically generated using paths in the final witness graph. The simulation is

performed using the generated testbench.

Claim 1 recites generating a witness graph, which may include different paths depending

on the property as set forth in the "wherein" clauses of the claim. Moreover, claim 1 recites

automatic generation of the testbench when the witness graph is not empty. As correctly pointed

out by the Examiner, *how* the witness graph which is used for the testbench, is generated, is not

the focus of the claim. A witness graph, which is generated in a completely different way but is

capable of comprising *different paths for testbench* or an empty witness graph as set forth in

claim 1, meets the claim language. Therefore, it is necessary and appropriate for the Examiner to

withdraw this rejection of claim 1 and claims 2-13.

The Examiner also alleges that without reciting pruning, any conventional automatic

testbench meets the limitations of claim 1 (see pages 4-5 of the Office Action). The Examiner is

respectfully requested to explain or provide an example as to how any automatic testbench

generation meets the recitations of generating a witness graph, generating a test bench and then

performing simulation using the testbench and other recitations of claim 1.

D. Claims 2 and 15 are definite

Next, the Examiner rejected claims 2 and 15 for reciting "generating a vector generator

module". In particular, the Examiner alleges that modules may be hardware or software and that

they already exist and therefore are not being generated (see page 5 of the Office Action).

Applicant respectfully points to page 8 of the Specification for an exemplary, non-limiting

embodiment of generating modules. For example, once the testbench is being generated (e.g. a

C or a Verilog program is executed), modules for vector generation and monitoring are

generated; then **using these generated modules** simulation may be performed. The module is

itself generated; the claim language means just what it says. The claims are in no way indefinite.

E. Claim 14 is definite

With respect to claim 14, the Examiner alleges that it is unclear what is meant by

"completely simulated". It is respectfully noted that one of ordinary skill in art would ascertain

the scope of the claim and would readily recognize what is meant by this term. For example, an

illustrative, non-limiting embodiment teaches that a path is completely simulated when a

conclusive result was reached or when the path has been fully expanded (see e.g., pages 27 and

29). Therefore, it is appropriate and necessary for the Examiner to withdraw this rejection to

claim 14.

F. Claim 18

Finally, with respect to claim 18, the Examiner alleges that it is indefinite for insufficient

antecedent basis (see page 6 of the Office Action). Applicant thanks the Examiner for pointing

out with particularity aspects of the claim thought to be indefinite. Applicant amends claim 18 to

remedy this minor informality. Therefore, the Examiner is respectfully requested to withdraw

this rejection in view of this self-explanatory claim amendment.

VIII.   Claim Rejection under 35 U.S.C. § 102(b)

The Examiner rejected claims 1, 15 and 16 under 35 U.S.C. § 102(b) as being allegedly

anticipated by Geist et al. ("Coverage-directed test generation using symbolic techniques," In

Proceedings of the International Conference on Formal Methods in CAD, pgs. 143-158, Nov.

1996), hereinafter "Geist". In addition, claim 16 is also rejected under 35 U.S.C. § 102(b) as

being allegedly anticipated by Gupta et al. ("Toward formalizing a validation methodology using

simulation coverage," Design Automation Conference, 1997. Proceedings of the 34th, June 9-

13, 1997, pgs. 740-745), hereinafter "Gupta". Applicant respectfully traverses these rejections

and respectfully request the Examiner to reconsider in view of the following comments.

Independent claim 1 includes a number of unique features not found in the cited

reference, such as: *generating a witness graph for one of said one or more correctness properties*

based on a deterministic analysis of said abstract model...generating a testbench automatically

*when said witness graph is not empty...*The Examiner asserts that claim 1 is directed to a method

of verification for a design and is anticipated by Geist. The Examiner asserts that Geist's

specification and/or implementation modeling is equivalent to generating a witness graph, as set

forth in claim 1, and that Geist's test generation is equivalent to automatic testbench when said

witness graph is not empty, as set forth in claim 1 (see page 7 of the Office Action). Applicant

respectfully disagrees. Applicant has carefully studied Geist's discussion of building an FSM

Model and test generation, which are not similar to generating a witness graph and automatic

testbench when the witness graph is not empty, respectively, as set forth in claim 1.

Geist teaches using formal verification technique along with simulation for functional

validation. Powerful abstraction mechanism is provided by which vector generation can be

applied to specific parts of the implementation that are the focus of verification. The abstraction

is achieved by portioning the implementation state variables into categories of interest. Next,

Geist teaches *departing from the traditional graph-algorithm model* for conformance testing;

instead, temporal logic assertions are used (§ 1, ¶ 4).

In particular, Geist teaches that a user identifies design functions to test (specification

modeling) and defines a finite state machine model that performs these functions to be tested

(implementation modeling). Any details not relevant to the desired function may be removed by

the user; thereby isolating manually the core design for the desired functions (§ 3.0, ¶2). Next,

Geist teaches generating tests (generate random vectors for testing) by using a translator and

concretizer. A translator is used to transform the core design into lower level tests (add detail,

information for inputs). Next, these lower level abstract tests are transformed into concrete

lower level tests by being converted into lower level language appropriate for simulations (§ 3,

¶¶ 5-7 and § 3.3).

Geist, however, *only teaches creating an abstract model* of the design by either

specification modeling <u>or</u> implementation modeling; both are performed *manually by the user*.

Next, this abstract model is used to generate vectors (tests) for simulation (translation and

concretization). Geist fails to teach or suggest *having a witness graph* for one of the correctness

properties based on the abstracted model. The abstract model is used directly for simulation.

In fact, Geist is discussed on page 10 of the Specification as a *related work*, which

teaches abstracting a model from the design description and generating simulation vectors. But

as noted on page 10, it *fails to further modify the abstraction model by generating a witness*

graph depending on the correctness of property of interest and based on this graph generate a

testbench. In short, Geist teaches having an abstracted model for generating simulation vectors

and fails to teach or suggest generating a witness graph which is used for automatic testbench.

Therefore, *generating a witness graph for one of said one or more correctness*

properties based on deterministic analysis of said abstract model and *generating a testbench*

automatically when said witness graph is not empty, as set forth in claim 1, is not suggested or

taught by Geist, which lacks any further modification of the abstraction model and instead

uses this abstraction model for vector simulation.

Moreover, it is respectfully noted that while Geist teaches providing counter examples to

the assertions; it *does not teach or suggest defining witnesses* when the property refers to

existential path qualification. The focus of Geist is on finding counter-examples (§ 3.2 "Test

Generation Efficiency). For at least these exemplary reasons, it is respectfully submitted that

independent claim 1 is patentably distinguishable from Geist. Therefore, the Examiner is

respectfully requested to reconsider and withdraw this rejection of independent claim 1.

Next, independent claim 15 among a number of unique features not found in the cited

references, recites: *a hardware description including correctness criteria expressed as a*

correctness property and *generating a witness graph based on said hardware description.* This

recitation is similar to the recitation of *generating a witness graph* as set forth in claim 1.

Similarly, claim 16 recites *generating a witness graph for one or more of said correctness*

properties. Since claims 15 and 16 contain features that are somewhat similar to the features

argued above with respect to claim 1, those arguments are respectfully submitted to apply with

equal force here. For at least substantially the same exemplary reasons, therefore, it is

respectfully requested that the Examiner withdraw this rejection of independent claims 15 and

16.

Next, the Examiner alleges that claim 16 is also anticipated by Gupta. Applicant

respectfully traverses this rejection as set forth below. Claim 16 recites, among a number of

other unique features not found in the prior art: *generating a witness graph for one or more of*

said correctness properties. The Examiner alleges that Fig. 2 of Gupta teaches this, but is

incorrect as a technical matter. Gupta's Fig. 2 is just an illustration of a *fragment of a test space*

of a test model and is not similar to a witness graph for one or more of said correctness

properties. In short, Gupta fails to teach or suggest having this fragment of a test space for one

or more correctness property.

Gupta is concerned with complete error coverage in hardware validation techniques.

Therefore, Gupta uses Fig. 2 to show the limitations of transition tours (§ 4.2, ¶ 1). Gupta fails

to teach or suggest *generating a witness graph for one or more correctness properties*. For at

least this exemplary reason, it is respectfully submitted that independent claim 16 is patentably

distinguishable from Gupta. Therefore, the Examiner is respectfully requested to reconsider and

withdraw this rejection of independent claim 16.

IX.   Claim Rejections under 35 U.S.C. § 103(a)

The Examiner rejected claim 1 as being obvious over Geist in view of Gupta, claims 2-3

as being obvious in view of Geist over US Patent No. 6, 182,258 to Hollander (hereinafter

"Hollander") and claim 4 as being obvious in view of Geist over Hollander and the references

cited by the Applicant. Applicant respectfully traverses these rejections and respectfully requests

the Examiner to reconsider in view of the following comments.

With respect to claim 1, it was already demonstrated that neither Geist nor Gupta meet all

the requirements of claim 1. In addition, there is no motivation to combine the references in the

manner suggested by the Examiner. In particular, the Examiner alleges that it would have been

obvious to combine Gupta and Geist because this would provide coverage of the abstract model

while ensuring that each test obeys the constraints (see page 11 of the Office Action). It is

respectfully pointed out that *Gupta has considered Geist's teaching* (see references: number 13

and § 3 of Gupta titled "related works") but yet, Geist's teachings were not incorporated into

Gupta, but instead they were dismissed by Gupta "most of these coverage metrics do not provide

a measure of the design error coverage". In short, there is no motivation to combine the

references in a manner suggested by the Examiner. Therefore, together, the combined teachings

of these references would not have (and could not have) led the artisan of ordinary skill to have

achieved the subject matter of claim 1.

With respect to claims 2-3, which depend upon claim 1 and stand rejected as being

obvious over Geist in view of Hollander, it was already demonstrated that Geist does not meet all

of the requirements of the independent claim 1. Hollander is relied upon only for its teaching of

generating vectors using random patterns and applying constraints to select the desirable ones (see

page 12 of the Office Action). Clearly, Hollander does not compensate for the above-identified

deficiencies of Geist. Together, the combined teachings of these references would not have (and could not have) led the artisan of ordinary skill to have achieved the subject matter of claim 1. Since claims 2-3 dependent upon claim 1, they may be patentable at least by virtue of their dependency.

With respect to claim 4, which also depends on claim 1 and stands rejected as being obvious over Geist in view of Hollander and the references cited in the specification, it was already demonstrated that Geist and Hollander do not meet all of the requirements of the independent claim 1. References cited in the specification are relied upon only for their teachings of various schemes for assigning priority (see page 13 of the Office Action). Clearly, the references cited in the specification do not compensate for the above-identified deficiencies of Geist and Hollander. Together, the combined teachings of these references would not have (and could not have) led the artisan of ordinary skill to have achieved the subject matter of claim 1. Since claim 4 depends upon claim 1, it is clearly patentable at least by virtue of its dependency.

X.   Allowable Subject Matter

The Examiner's indication that claim 17 contains allowable subject matter and would be allowed if rewritten in the independent form including all the limitations of the base claim is gratefully noted. Applicant respectfully holds the rewriting of claim 17 in abeyance until the arguments presented with respect to independent claim 16 have been reconsidered.

XI.   Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the

Examiner feels may be best resolved through a personal or telephone interview, the Examiner is

kindly invited to contact the undersigned attorney at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue

Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any

overpayments to said Deposit Account.

Respectfully submitted,
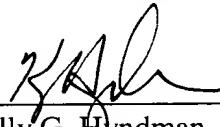
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